



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/084,214	02/25/2002	Brian Dennis McKean	IBMS.038US01(0549)	5101
7590	04/06/2006		EXAMINER	
Chambliss, Bahner & Stophel, P.C. 1000 Tallan Building Two Union Square Chattanooga, TN 37402			TANG, KENNETH	
			ART UNIT	PAPER NUMBER
			2195	

DATE MAILED: 04/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/084,214	MCKEAN ET AL.
	Examiner	Art Unit
	Kenneth Tang	2195

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 27 December 2005.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-42 is/are pending in the application.
 - 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-42 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 12/27/05 is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

1. Applicant's arguments are in response to the Amendment filed on 12/27/05. Applicant's arguments have been fully considered but are not found to be persuasive.
2. Claims 1-42 are presented for examination.

Response to Arguments

3. During patent examination, the pending claims must be "given their broadest reasonable interpretation consistent with the specification." *In re Hyatt*, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000). Applicant always has the opportunity to amend the claims during prosecution, and broad interpretation by the examiner reduces the possibility that the claim, once issued, will be interpreted more broadly than is justified. *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-51 (CCPA 1969).

4. *Applicant argues throughout the Remarks that US Patent No. 6,862,668, Simpson, nor Pecone suggest a controller of the plurality of controllers initiates a task to be performed, wherein the controller initiating the task establishes a task coordination data object shared by the plurality of controllers.*

In response, the Examiner respectfully disagrees. The CPU processors 71, 72, 73, or 74 are the plurality of controllers, where one of those processors is selected. The controller initiates the task upon receipt of a command word from master processor 60. The task coordination data object shared by the plurality of controllers is the TASK interrupt vector (*see Simpson, col. 14, lines 57-63*).

5. *Applicant argues that Moriyama does not establish a task coordination data object that is shared by other controllers.*

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). This feature was shown to be taught in the reference of Simpson (see above). Motivation has been provided to combine Simpson and Moriyama. Applicant does not argue the motivation in the Response.

6. *Applicant argues that Moriyama does not teach a task being broken down into partitioned tasks and an object that is shared between controllers that allows a controller to complete an uncompleted partitioned task.*

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). The feature of an object shared between a plurality of controllers to complete a task was shown to be taught in the reference of Simpson (see above). Motivation has been provided to combine Simpson and Moriyama. Applicant does not argue the motivation in the Response. Moriyama teaches the task being broken down into partitioned tasks based on various states such as a ready state, a state of execution (IN PROGRESS) state, an end (COMPLETE) state, etc. (*col. 9, lines 45-67 through col. 10, lines 1-14*). In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "complete an uncompleted task") are not recited in the rejected claim(s). Although the claims

are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

7. *Applicant argues regarding claim 1, 12, 23, 34, and 42, that Studdard fails to suggest a free controller selecting a partition of the task available for processing as indicated by the states represented in the task coordination data object.*

In response, the rejections were of claims 1, 12, 23, 34, and 42 did not even use Studdard as a reference. It was already shown above that in claim 1, 12, 23, 34, and 42, the features suggesting a free controller selecting a partition of the task available for processing as indicated by the states represented in the task coordination data object, is taught in Simpson and Moriyama.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-11 and 23-42 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,862,668 B2 in view of Moriyama et al. (hereinafter Moriyama) (US 6,466,991 B1).

8. As to claim 1, U.S. Patent No. 6,862,668 B2 teaches a mass storage controller system, comprising:

a plurality of controllers for controlling an array of storage devices (multi-controller storage device) (claim 1, lines 2-3), each of the plurality of controllers comprising:

a CPU for controlling the operation of a controller (*inherent in the controller*);
program memory, coupled to the CPU, for storing program instructions

and variables for the operation of the CPU (*claim 1, line 16*)); and

cache memory, coupled to the CPU, for storing information related to the array of storage devices (*claim 1, line 1*);

9. U.S. Patent No. 6,862,668 B2 also teaches establishing by the initiating controller a task coordination by the multiple controllers (*claim 1, lines 5-19*). U.S. Patent No. 6,862,668 B2 fails to explicitly teach using data objects that represent discrete partitions of the task to be performed and states for each partition. However, Moriyama teaches a processor/controller that uses data objects that are discretely partitioned into various states of tasks such as a ready state, a state of execution (IN PROGRESS) state, an end (COMPLETE) state, etc. (*col. 9, lines 45-67 through col. 10, lines 1-14*). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the feature of using data objects that represent discrete partitions of the task to be performed and states for each partition to the existing task communication/controller system because using data objects and an object-oriented technique would improve communication in the data system (*col. 1, lines 10-16 and 56-65*).

10. Claims 2-11, 23-42 are rejected for the same double patenting reasons as stated above.

11. **Claims 12-22 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 5 of U.S. Patent No. 6,862,668 B2 in view of Moriyama et al. (hereinafter Moriyama) (US 6,466,991 B1).**

12. As to claim 12, U.S. Patent No. 6,862,668 B2 teaches a mass storage array subsystem, comprising:

a plurality of storage devices (*claim 5, line 2*);

a backplane adapted to couple to said plurality of storage devices (*claim 5, lines 3-4*); and

a plurality of controllers, coupled to the backplane, for controlling the plurality of storage devices, the plurality of controllers having a first interface to couple to a host system and a second interface adapted to couple to said backplane to communicate with said plurality of storage devices (*claim 5, lines 5-10*);

wherein each of the plurality of controllers comprise a CPU for controlling the operation of a controller, program memory for storing program instructions and variables for the operation of the CPU and cache memory for storing information related to the array of storage devices, and wherein a controller of the plurality of controllers initiates a task to be performed (*claim 5, lines 11-28*).

13. U.S. Patent No. 6,862,668 B2 fails to explicitly teach using data objects that represent discrete partitions of the task to be performed and states for each partition. However, Moriyama

teaches a processor/controller that uses data objects that are discretely partitioned into various states of tasks such as a ready state, a state of execution (IN PROGRESS) state, an end (COMPLETE) state, etc. (*col. 9, lines 45-67 through col. 10, lines 1-14*). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the feature of using data objects that represent discrete partitions of the task to be performed and states for each partition to the existing task communication/controller system of Pecone because using data objects and an object-oriented technique would improve communication in the data system (*col. 1, lines 10-16 and 56-65*).

14. Claims 13-22 are rejected for the same double patenting reasons as stated above.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

15. Claims 12-41 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention:

- a. In claim 12, there is no relationship made between the "host" and the "backplane" or the "second interface" associated with the "backplane". It is not clear whether or not communication is involved.
- b. In claims 23 and 34, there is no relationship made between "cache locking" (in preamble) to anything else in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

16. Claims 1-8, 10-11, 23-30, and 32-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Simpson et al. (hereinafter Simpson) (US 6,185,629 B1) in view of Moriyama et al. (hereinafter Moriyama) (US 6,466,991 B1).

17. As to claim 1, Simpson teaches a mass storage controller system, comprising:
a plurality of controllers for controlling (*col. 14, lines 57-63, col. 17, lines 13-32, Fig. 2, items 60, 71-74*) an array of storage devices (*Fig. 2, items 11-15, 21-40*), each of the plurality of controllers comprising:
a CPU for controlling the operation of a controller (*col. 14, lines 57-63, col. 17, lines 13-32, Fig. 2, items 60, 71-74*);
program memory, coupled to the CPU, for storing program instructions and variables for the operation of the CPU (*col. 14, lines 57-63, col. 17, lines 13-32, Fig. 2, items 60, 71-74*); and
cache memory, coupled to the CPU, for storing information related to the array of storage devices (*col. 14, lines 57-63, col. 17, lines 13-32, Fig. 2, items 60, 71-74*);

18. Simpson also teaches establishing by the initiating controller a task coordination by the multiple controllers (*col. 14, lines 57-63, col. 17, lines 13-32, Fig. 2, items 60, 71-74*). Simpson fails to explicitly teach using data objects that represent discrete partitions of the task to be performed and states for each partition. However, Moriyama teaches a processor/controller that uses data objects that are discretely partitioned into various states of tasks such as a ready state, a state of execution (IN PROGRESS) state, an end (COMPLETE) state, etc. (*col. 9, lines 45-67 through col. 10, lines 1-14*). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the feature of using data objects that represent discrete partitions of the task to be performed and states for each partition to the existing task communication/controller system because using data objects and an object-oriented technique would improve communication in the data system (*col. 1, lines 10-16 and 56-65*).

19. As to claim 2, Moriyama teaches wherein the state indicates whether a partition is READY, IN PROGRESS, or COMPLETE (*col. 9, lines 45-67 through col. 10, lines 1-14*).

20. As to claim 3, Moriyama teaches wherein a controller selects a partition by examining the partitions in a READY state and selecting at least one partition in the READY state to operate on (*col. 9, lines 45-67 through col. 10, lines 1-14*).

21. As to claim 4, Moriyama teaches wherein a partition is in an IN PROGRESS state during processing (*col. 9, lines 45-67 through col. 10, lines 1-14*).

22. As to claim 5, Moriyama teaches wherein a controller sets the partition selected for processing to a COMPLETE state upon completion of processing for a partition (*col. 9, lines 45-67 through col. 10, lines 1-14*).

23. As to claim 6, Moriyama teaches wherein a controller selects a partition by examining the partitions in a READY state and selecting at least one partition in the READY state to operate on (*col. 9, lines 45-67 through col. 10, lines 1-14*).

24. As to claim 7, Moriyama teaches wherein a partition is in an IN PROGRESS state during processing (*col. 9, lines 45-67 through col. 10, lines 1-14*).

25. As to claim 8, Moriyama teaches wherein a controller sets the partition selected for processing to a COMPLETE state upon completion of processing for a partition (*col. 9, lines 45-67 through col. 10, lines 1-14*).

26. As to claim 10, Moriyama teaches wherein the initiating controller is notified when all partition states are COMPLETE and performs whatever completion actions are required (*col. 9, lines 45-67 through col. 10, lines 1-14*).

27. As to claim 11, Moriyama teaches wherein the task coordination data object includes information about an operation to be performed and a data set to be operated on (*col. 9, lines 45-67 through col. 10, lines 1-14*).

28. As to claim 23, Simpson teaches a method for cooperative distributed task management in a storage subsystem with multiple controllers, comprising:

initiating by an initiating controller a task to be performed (*col. 14, lines 57-63, col. 17, lines 13-32, Fig. 2, items 60, 71-74*);

establishing by the initiating controller a task coordination by the multiple controllers (*col. 14, lines 57-63, col. 17, lines 13-32, Fig. 2, items 60, 71-74*); and

selecting by a free controller a partition of a task available for processing as indicated by the states (transfer controller 80) (*col. 11, lines 15-21, col. 12, lines 50-54*).

29. Simpson fails to explicitly teach using data objects that represent discrete partitions of the task to be performed and states for each partition. However, Moriyama teaches a processor/controller that uses data objects that are discretely partitioned into various states of tasks such as a ready state, a state of execution (IN PROGRESS) state, an end (COMPLETE) state, etc. (*col. 9, lines 45-67 through col. 10, lines 1-14*). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the feature of using data objects that represent discrete partitions of the task to be performed and states for each partition to the existing task communication/controller system because using data objects and an object-oriented technique would improve communication in the data system (*col. 1, lines 10-16 and 56-65*).

30. As to claim 24, Moriyama teaches further comprising indicating a state of a partition as being READY, IN PROGRESS, or COMPLETE (*col. 9, lines 45-67 through col. 10, lines 1-14*).

31. As to claim 25, Moriyama teaches wherein the selecting by a free controller is performed by examining the partitions in a READY state and selecting at least one partition in the READY state to operate on (*col. 9, lines 45-67 through col. 10, lines 1-14*).

32. As to claim 26, Moriyama teaches wherein a partition is in an IN PROGRESS state during processing (*col. 9, lines 45-67 through col. 10, lines 1-14*).

33. As to claim 27, Moriyama teaches further comprising setting by a controller a partition selected for processing to a COMPLETE state upon completion of processing for the partition (*col. 9, lines 45-67 through col. 10, lines 1-14*).

34. As to claim 28, Moriyama teaches wherein the selecting by a free controller is performed by examining the partitions in a READY state and selecting at least one partition in the READY state to operate on (*col. 9, lines 45-67 through col. 10, lines 1-14*).

35. As to claim 29, Moriyama teaches wherein a partition is in an IN PROGRESS state during processing (*col. 9, lines 45-67 through col. 10, lines 1-14*).

36. As to claim 30, Moriyama teaches further comprising setting by a controller a partition selected for processing to a COMPLETE state upon completion of processing for the partition (*col. 9, lines 45-67 through col. 10, lines 1-14*).

37. As to claim 32, Moriyama teaches further comprising notifying the initiating controller when all partition states are complete and performing completion actions that are required (*col. 9, lines 45-67 through col. 10, lines 1-14*).
38. As to claim 33, Moriyama teaches wherein the task coordination data object includes information about an operation to be performed and a data set to be operated on (*col. 9, lines 45-67 through col. 10, lines 1-14*).
39. As to claims 34-41, they are rejected for the same reasons as stated in the rejections of claims 2-6 and 10-11.
40. As to claim 42, it is rejected for the same reasons stated in the rejection of claim 1.
41. **Claims 9 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Simpson et al. (hereinafter Simpson) (US 6,185,629 B1) in view of Moriyama et al. (hereinafter Moriyama) (US 6,466,991 B1), and further in view of Stuttard et al. (hereinafter Stuttard) (US 2002/0174318 A1).**
42. As to claims 9 and 31, Simpson and Moriyama fails to explicitly teach wherein the states provide a semaphore-mechanism for allowing a controller to ascertain whether to acquire control

over a partition. However, Stuttard teaches using a semaphore controller for a data processing apparatus (*page 7, [0140]-0142*). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the references of Stuttard with Simpson and Moriyama because this would allow for synchronization of threads and to increase the control of accesses to resources (*page 7, [0140]-0142*).

43. Claims 12-19, and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pecone (US 2003/0065836 A1) in view of Moriyama et al. (hereinafter Moriyama) (US 6,466,991 B1).

44. As to claim 12, Pecone teaches a mass storage array subsystem, comprising:
a plurality of storage devices (at least one storage device) (*page 2, [0013]*);
a backplane, coupled to the plurality of storage devices, adapted (by interface modules) to couple to said plurality of storage devices (*page 2, [0013]*); and
a plurality of controllers (at least two controller memory modules), coupled to the backplane, for controlling the plurality of storage devices, the plurality of controllers having a first interface coupled to a host system and a second interface adapted coupled to said backplane to communicate with said plurality of storage devices (two channel interface modules, which are connected to the passive backplane, the host computer and the storage devices) (*page 2, [0013]*);
wherein each of the plurality of controllers comprise a CPU for controlling the operation of a controller (each controller includes a CPU subsystem 50), program memory for storing program instructions and variables for the operation of the CPU (memory 54 to store data and

information such as for the control logic 58, [0006]) and cache memory for storing information related to the array of storage devices (cache memory and array of disks) (*page 1, [0005]-[0006]*), and wherein a controller of the plurality of controllers initiates a task to be performed (CPU performs tasks) (*page 1, [0006]*).

45. Pecone fails to explicitly teach using data objects that represent discrete partitions of the task to be performed and states for each partition. However, Moriyama teaches a processor/controller that uses data objects that are discretely partitioned into various states of tasks such as a ready state, a state of execution (IN PROGRESS) state, an end (COMPLETE) state, etc. (*col. 9, lines 45-67 through col. 10, lines 1-14*). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the feature of using data objects that represent discrete partitions of the task to be performed and states for each partition to the existing task communication/controller system of Pecone because using data objects and an object-oriented technique would improve communication in the data system (*col. 1, lines 10-16 and 56-65*).

46. As to claims 13-19 and 21-22, these limitations are taught in Moriyama as shown in the rejections of claims 2-8 and 10-11.

47. **Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Simpson et al. (hereinafter Simpson) (US 6,185,629 B1) in view of Moriyama et al. (hereinafter**

Moriyama) (US 6,466,991 B1), and further in view of Stuttard et al. (hereinafter Stuttard) (US 2002/0174318 A1).

48. As to claim 20, Pecone and Moriyama fails to explicitly teach wherein the states provide a semaphore-mechanism for allowing a controller to ascertain whether to acquire control over a partition. However, Stuttard teaches using a semaphore controller for a data processing apparatus (*page 7, [0140]-0142*). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the references of Stuttard with Pecone and Moriyama because this would allow for synchronization of threads and to increase the control of accesses to resources (*page 7, [0140]-0142*).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth Tang whose telephone number is (571) 272-3772. The examiner can normally be reached on 8:30AM - 6:00PM, Every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kt
3/31/06


MENG-AI AN
SUPERVISORY PATENT EXAMINER